ing switch mode power amplifiers, linear power amplifiers, etc. Therefore, although the following illustrative embodiments pertain especially to switch mode power amplifiers, it should be recognized that various other embodiments are equally embraced by the present disclosure. Referring now to Figure 1, a diagram is shown of a saturation prevention circuit that may be used with an exemplary embodiment of the invention. (The saturation prevention circuit itself is the subject of U.S. Patent Application 09/738,691, entitled SATURATION PREVENTION AND AMPLIFIER DISTORTION REDUCTION, filed December 15, 2000 and incorporated herein by reference.) A transistor Q1 is coupled to a power source, Vbat, and to a load L.

In the present application, the load L is an RF amplifier as illustrated in Figure 3 and described in greater detail in U.S. Patent Application 09/247,095, entitled HIGH-EFFICIENCY MODULATING AMPLIFIER, filed February 9, 1999 and incorporated herein by reference. Briefly, the amplifier is part of a polar (as opposed to I-Q) amplifier architecture in which separate amplitude and phase paths are provided. The phase path is coupled to an RF input of the amplifier. The amplitude path is coupled to the power supply input of the amplifier. In the embodiment of Figure 3, therefore, circuitry 300 functions as an AM modulator.

Referring again to Figure 1, in this configuration, the transistor Q1 is a bipolar transistor having an emitter terminal coupled to Vbat and a collector terminal coupled to the load L. The collector terminal is also coupled to a resistive network comprising series-connected resistors R1 and R2 coupled to ground. A voltage occurring at node *A* between the resistors R1 and R2 is proportional to the voltage applied to the load L. A resistor R3 is coupled between the emitter terminal and the base terminal of the transistor Q1. The combination of the resistors R1-R3 allows the gain of the transistor Q1 to be set.

An operational amplifier (op amp) 101 is provided as part of a feedback circuit used to control the transistor Q1 and thus set a voltage applied to the load L.